ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING RECEIVER

CROSS-REFERENCE

[0001] This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/577,602 filed on June 8, 2004, which is incorporated herein by reference.

BACKGROUND AND SUMMARY OF THE DISCLOSURE

[0002] The present invention relates generally to communication receivers and, more specifically, to orthogonal frequency division multiplexing (OFDM) receivers.

[0003] The following disclosure will describe a digital video broadcasting (DVB) receiver for digital terrestrial television (DTV). The concepts are equally applicable to any other channels of transmission of DTV receivers and to other receivers or standards using orthogonal frequency division multiplexing (OFDM). These may include but not be limited to wireless standards worldwide such as wireless LAN 802.11a and g, HIPERLAN/2, Digital Audio Broadcasting (DAB), Digital Video Broadcasting Terrestrial (DVB-T), Digital Video Broadcasting for handheld (DVB-H), 802.16 Broadband Wireless Access, etc

[0004] The European terrestrial DTV standard DVB-T (ETS 300 744) is based on COFDM technologies to combat multipath fading. *See* ETSI EN 300 744 V.1.4.1 "Digital Video Broadcasting (DVB): Framing Structures, channel coding, and modulation for digital terrestrial television." It specifies two operational modes:

1) A 2K mode based on 2048 FFT and having 1,705 carriers per OFDM symbol; and
2) An 8K mode based on 8192 FFT and having 6,817 carriers per OFDM symbol.

[0005] Figure 1 shows a block diagram for a typical DVBT receiver. The digital signal processing for a DVBT receiver can be partitioned into three portions. The first portion 10 includes an RF front end 12 , and A/D converter 14, an OFDM demodulator 16, a demodulation 18 and a pilot and TPS decoder 19. This receiver front-end signal processing portion performs receiver training, including various synchronization and channel estimation and OFDM demodulation. The second portion 20 is the DVBT receiver back-end signal processing block. It performs DVBT inner channel decoding and outer channel decoding. The third portion 30 is a MPEG Decoder. An example is shown in US Patent 6,359,938.

[0006] Due to computational complexity and high MIPs required for the DVBT receiver, until recently, DVBT receivers have been implemented in hardware using ASICs. In the case of multi-protocol communication systems, the hardware implementation becomes

less attractive due to extra chip cost and PC board area consumed. In this disclosure, an improved software implementation of a DVBT receiver is described. In this design, all functions associated with the DVBT receiver may be implemented in software in the Sandbridge Technologies Multithreaded SB9600 processor. The device may be used in hand-held devices, such as mobile phones and PDAs.

[0007] The receiver includes an A/D converter for converting receiver analog signals to a digital signal data stream, wherein the digital signal data stream includes symbols separated by guard segments. The receiver also includes an I/Q demodulator for producing a first set of complex I and Q components from the digital signal data stream and a guard segment length detector using the first set of I and Q components. It further includes an extractor for identifying and removing the guard segments of the detected length from the digital signal data stream and an FFT demodulator for demodulating the symbols of the digital signal data stream to produce second sets of complex I and Q components.

[0008] The FFT demodulator is an orthogonal frequency division multiplexing demodulator and the receiver may be a digital video broadcasting receiver. The FFT demodulator demodulates two symbols at one time to produce the second sets of complex I and Q components. A processor is programmed to operate as the I/Q demodulator, the guard segment length detector, the extractor, and the FFT demodulator. The FFT demodulator is an orthogonal frequency division multiplexing demodulator, and the receiver may be a digital video broadcasting receiver.

[0009] The receiver may include at least two antennas each connected to a respective receiver front-end and A/D converter. The at least two antennas are orthogonally positioned and the receiver front-end includes a phase shifter.

[00010] The receiver includes a first carrier signal offset estimator and a first symbol synchronizing signal generator, each using the first set of I and Q components, to estimate the offset of the carrier signal and adjusting the A/D converter and to generate a symbol synchronizing signal for the extractor, respectively, at least during an initialization phase of the receiver. The I/Q demodulator, the guard segment length detector, the first carrier signal offset estimator, and the first symbol synchronizing signal generator operate only during the initialization phase of the receiver. The receiver includes a second carrier signal offset estimator and a second symbol synchronizing signal generator, each using the second sets of I and Q components from the FFT demodulator, to estimate the offset of the

carrier signal and adjusting the A/D converter and to generate a symbol synchronizing signal for the extractor, respectively, at least after an initialization phase of the receiver.

[00011] These and other aspects of the present disclosure will become apparent from the following detailed description of the disclosure, when considered in conjunction with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[00012] Figure 1 is a block diagram of a digital video broadcasting terrestrial receiver, according to the prior art for a single input single output (SISO) system.

[00013] Figure 2 is a block diagram of the orthogonal frequency division multiplexing demodulator of the prior art.

[00014] Figure 3 is a block diagram of an orthogonal frequency division multiplexer demodulator, according to the present disclosure.

[00015] Figure 4 shows an off-frequency division multiplexer symbol extraction, according to the present disclosure.

[00016] Figure 5 is a block diagram of a digital video broadcasting terrestrial receiver, according to the present disclosure for a multiple input multiple output (MIMO) system.

[00017] Figure 6 is a graph of the Rayleigh fading of a MIMO system as a function of the number of receivers.

[00018] Figure 7 is a block diagram of a receiver's front end using two mutually orthogonal antennas.

[00019] Figure 8 is a diagram of the two antennas of Figure 7 on a device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[00020] A digital video broadcasting/terrestrial receiver of the prior art is illustrated in Figure 1. The first portion 10 includes an RF receiver front end 12 for receiving UHF and VHF signals from antenna 11 and A/D converter 14. The signals are then provided to an OFDM demodulator 16. The output of the OFDM demodulator 16 is connected to Demodulator 18 and Pilot and TPS decoder 19. These block performs receiver training, including various synchronization and channel estimation and the OFDM demodulation.

[00021] The various signals (including, for example, the complex I and Q components of the digital signal) are provided to the receiver back-end signal processing block 20. This includes inner-deinterleaver 21, a Viterbi decoder 22, an outer deinterleaver 24, an RS decoder 65 and an energy disperse removal 28. The output of the back-end signal processing block 20 is provided to an MPEG decoder/demultiplexer portion 30. The output signals may be, for example, video services, audio services and data services.

[00022] A more detailed description of the Front end 10 is shown in Figure 2. The RF processed analog signal from RF front-end receiver 12 is provided to the A/D converter 14. The digital signal is provided to a sampling rate correction interpolation and decimation process 52. The output of 52 is then provided to a digital I/Q generator 54, which generates the complex I and Q components or signals required for the OFDM demodulator 64. The complex I/Q signal is provided to the initial course symbol synchronization portion 56 and to the guard segment length detector and coarse frequency offset estimator 58. The carrier frequency offset may be corrected digitally by properly de-rotating the I/Q signals at the frequency offset correction 60. This uses the initial coarse frequency offset estimation of 58. The guard segment length can be detected at 58 and the corresponding guard segment period removed at 62 From the I/Q signal stream.

[00023] The digital signal data stream (without the guard segments) is then processed by the FFT demodulator 54, which performs a fast Fourier Frequency Transformation (FFT) on the complex I/Q signals. A 2048 point complex FFT is performed for the 2K mode, and a 8192 point complex FFT is performed for an 8K mode. These are the modes used in the previously mentioned standard.

[00024] The demodulated OFDM symbols, as complex I/Q components, are provided to the TPS decoder 66, the channel correction 68 and channel estimation 70. The channel correction 68, having input also from the channel estimation 70, provides an output for the QAM demapper 72, which provides the output to the receiver back-end processing block 20. The I/Q signals out of the OFDM demodulator 64 are also provided to the SNR estimator 74, which provides input to the Viterbi decoder 76. The demodulated I/Q signals are also provided to the post-FFT frequency offset estimation 78, which provides a feedback to the frequency offset correction portion 60. The demodulated I/Q signals are also provided to the post-FFT sampling rate estimator 80, which provides a feedback signal to the sampling rate correction interpolation and decimation portion 52. The demodulated I/Q signals are provided to the post-FFT symbol timing estimation tracking portion 82, which provides a feedback to the guard period removal 62.

[00025] It should also be noted that the post-FFT sampling rate estimation circuit 80 also provides a signal to the voltage control oscillator 84, which provides a signal back to the RF receiver 12 for the adjustment of the final LO frequency of the analog receiver circuit 12. and to the A/D converter 14 for adjusting the A/D sampling rate.

[00026] The digital generation of the complex I/Q signals at 54 produces computational complexity and high MIPs required for the receiver.

[00027] The present disclosure, as will be noted below, only uses the digital complex I/Q signal generation during the initialization phase required for the initial symbol synchronization, guard length detector and initial coarse frequency offset estimation. Subsequently, the operation of the OFDM demodulator 64 is performed in such a way as to produce the required demodulated complex I/Q components without a digital I/Q generator 54.

[00028] A modified OFDM front-end signal processing architecture is shown in Figure 3. The receiver performs 2*N real input FFT (where N = 2048 for 2K mode and N = 8192 for 8K mode) for each received OFDM symbol. Further, the receiver can process two OFDM symbols per processing so that two 2*N real input FFT can be computed at the cost of one 2*N complex input FFT. Compared to the conventional DVBT OFDM front-end signal processing architecture of Figure 2, the present architecture of Figure 3 renders all the MIP intensive preprocessing before FFT demodulation unnecessary after initialization.

[00029] Although digital I/Q generation is initially required for the initial coarse symbol synchronization block 56 and the guard length detection/coarse fractional carrier frequency offset estimation block 58, this is only run once in the initial startup of our all software DVBT receiver, and it has the whole digital signal processor MIP resource available for its use after initialization.

[00030] The DVBT signal occupies a bandwidth of approximately 7.61 MHz. The signal modulated onto a center carrier is real as defined in the DVB standard. However, complex representation is required for the baseband DVBT signal. This is due to the fact that the DVBT baseband spectrum is not symmetrical around the middle frequency. This is the reason why MIP intensive preprocessing is required for generating the I/Q complex signals in conventional DVBT receiver. However, if the DVBT signal is kept in passband for FFT input, then the FFT input can be real, so that no I/Q generation would be required.

[00031] Further, the final stage LO and A/D sampling rate have to be carefully chosen to avoid any expensive interpolation and decimation that are sometimes required in conventional DVBT receiver. For 2K mode, the carrier spacing is f = 4464 Hz, and the sampling rate fs has to be exactly 2*2048*f = 18.284544 MHz. The final LO frequency f_LO has to be set exactly as: fs = 4 * f_LO.

[00032] For 4K mode, the carrier spacing is f = 2232 Hz, and the sampling rate fs has to be exactly 2*4096*f = 18.284544 MHz. The final LO frequency f_LO has to be set exactly as: fs = 4 * f_LO.

[00033] The above sampling rate fs and final LO frequency setting should also work for the 8K mode since the carrier spacing is now f = 1116 Hz, the sampling rate fs should be exactly 2*8192*f = 18.284544MHz, and the final LO frequency should be: fs = 4 * f_LO.

[00034] The elements of Figure 3 have the same functions or related functions as those of Figure 2. The analog signal from the receiver 12 is provided to A/D converter 14. The output of the A/D converter 14 is provided to the digital I/Q generator 54, as well as to the guard period removal 62. This distinguishes Figure 3 from Figure 2, wherein the guard period removal section 62 receives the digitally generated I/Q signal after frequency offset correction. The digital I/Q signals are provided to the initial coarse symbol synchronization portion 56 and the guard length detector and coarse frequency offset estimator 58. The detector and initial coarse frequency offset estimation 58 are provided to the guard period removal section 62.

[00035] The output of the guard period removal 62 is a digital stream and is provided to the OFDM FFT demodulator 64. As distinguished from Figure 2, this is not I/Q complex symbols but merely the digital signal data stream without the guard period. In Figure 3, as previously mentioned, the OFDM demodulator 64 processes two symbols at a time and produces (without the digital I/Q generation 54) the complex I/Q components.

[00036] These I/Q components are provided to the TPS decoder 66, the channel correction 68, the channel estimation 70, the SNR estimation 74, the post-FFT frequency offset estimation 78 and the post-FFT symbol timing estimation tracking 82. As in Figure 2, the channel correction 68 also receives signals from the channel estimation 70 and provides inputs to the QAM demapper 72. The SNR estimation 74 provides input to the Viterbi decoder 76. The post-FFT frequency offset estimation 78 provides a feedback signal to the voltage control oscillator VCXO 84, which provides the sampling rate signal to A/D converter 14, as well as a feedback signal to the RF receiver 12. The voltage control oscillator 84 also receives an initial frequency offset estimation from the initial coarse frequency offset estimator 58. The post-FFT symbol timing estimation tracking 82 provides a feedback signal to the guard period removal portion 62, as in Figure 2.

[00037] While the initial coarse symbol synchronization portion 56 and the guard length detector and initial coarse frequency offset estimation 58 are only performed during the initialization, as in Figure 2, the digital I/Q generation 54 is also only performed in the initialization stage. It should be noted that the I/Q or demodulator 54, the guard segment length detector and initial coarse frequency offset estimation 58, the initial coarse symbol

synchronization 56, the guard period removal 62 and the OFDM demodulator are all performed in software.

[00038] Figure 4 shows how OFDM symbols are extracted from A/D input signal data stream. Let the A/D input data stream sampling at fs be stored in a buffer called rx_in. Buffer holding rx_in should be large enough to hold more than two OFDM symbol worth of data samples, including all possible guard lengths. The rx_in read pointer rx_in_rd is controlled by the symbol synchronization algorithm and should point to the starting point of the current OFDM symbol. As depicted in Figure 4, two 2N points are extracted from the input signal stream for symbol 1 and symbol 2. It is well known that one can perform two 2N point real input FFT at the cost of one complex input FFT. Two OFDM symbols are processed at one time to produce I/Q without the intensive processing required by the I/Q demodulator/generator portion 54.

[00039] A MIMO OFDM receiver as an extension of the SISO by adding more receiver paths is illustrated in Figure 5. Each receiver path requires a separate set of RF antenna 11 and analog front-end circuitry and a separate signal processing channel in the same or separate side band digital signal processor depending on the volume of required computations. The front-end processed signal from the plural front-end signal processing block 10 are combined at 90 and provided as a single input to the back-end signal processing block 20 Each receiver signal processing channel must perform separate timing synchronization, frequency offset estimation, correction and channel estimation. The SISO DVB-T receiver of figures 1-3 performs poorly in the presence of NLOS (No-Line Of Sight) radio channel that can be modeled as Rayleigh fading. The SNR/BER improvement in MIMO-OFDM receiver of figure 5 is obtained by coherently combining the received signal from multiple receiver branches.

[00040] Figure 6 shows the performance improvement for MIMO-OFDM receiver with receiver spatial diversity. The simulation is set to 64 QAM mode, Rate ½, and portable Rayleigh fading channel model conforming to ETSI EN 300 744 V1.4.1 (2001-01). The plot shows SNR (at which the DVB-T receiver will be able to achieve QEF conditions) improvement from two, three and four receiver antennas. Generally speaking, more antennas will provide better SNR improvement at the cost of increased receiver complexity.

[00041] From the performance shown in Figure 6, by adding a second receiver the gain increases with 2.3 dB while adding three more receivers the gain will increase by 5.2 dB for the Ricean channel fading case. Adding more than two receivers, in addition to the

associated increased cost, there is also another undesired phenomenon, namely the mutual coupling of the antennas. In order to uncouple the antennas an uncoupling network needs to be added to the front end. Therefore, the gain achieved by adding more channels will be mainly lost by the added insertion loss. A good compromise will be to use only to receivers with mutually orthogonal antennas as illustrated in Figures 7 and 8.

[00042] In Figure 7, the RF signal coming from the antennas 11A and 11B are amplified by booster 92 and than fed into a phase shifter 94 controlled by the digital signal processor. The phase shifter 94 will shift the incoming waveform by an angle determined by the digital signal processor, such that the signals from the two antennas are combined coherently. The phase shifted signals are provided to the A/D converter 14 via matching circuit 96

[00043] Figure 8 shows the placement of the two antennas 11A and 11B on the hand held device 100. The antennas are orthogonally positioned.

[00044] Although the present disclosure has been described and illustrated in detail, it is to be clearly understood that this is done by way of illustration and example only and is not to be taken by way of limitation. The scope of the present disclosure is to be limited only by the terms of the appended claims.